

In the Claims

Please cancel claims 16, 18 and 22-29, and amend claims 15, 17 and 19 as shown.

1-7. (cancelled)

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8. (previously amended) A method, comprising:
using a conversion table to translate a first address from a graphics controller to a second address to a memory; and
using the conversion table to translate a third address from a bus controller to a fourth address to the memory;
wherein the second address has a greater number of bits than the first address and the fourth address has a greater number of bits than the third address .
9. (previously amended) The method of claim 8, wherein said using the conversion table to translate the third address includes using a translation lookaside buffer.
- 10-11. (cancelled)
12. (previously amended) The method of claim 8, wherein said using the conversion table to translate the third address includes:
comparing a first portion of the third address with entries in a first table;

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Contd.

if the first portion matches a particular one of the entries in the first table,
combining a value associated with the particular one with a second portion
of the third address to form the fourth address.

13. (previously amended) The method of claim 12, further comprising:
if the first portion does not match any of the entries in the first table, referring to
a second table to translate the third address.
14. (previously amended) The method of claim 13, wherein:
said comparing includes comparing the first portion of the third address with
entries in the first table in an input-output controller; and
said referring to the second table includes referring to the second table in main
memory.
15. (currently amended) An apparatus, comprising:
a translation lookaside buffer coupled to an input register and an output register;
control logic coupled to the translation lookaside buffer, the input register, and the
output register;
wherein the control logic is to compare a first portion of an initial address from a
bus controller in the input register with entries in the translation lookaside
buffer; and if a matching entry is found, to combine a first value
associated with the matching entry with a second portion of the initial
address to form a first translated address having a greater number of bits

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Cmtl.

than the initial address and hold the first translated address in the output register;

wherein the control logic is further to access a table in memory if the matching entry is not found, find a second value in the table associated with the first portion, combine the second value with the second portion to form a second translated address having a greater number of bits than the initial address, and hold the second translated address in the output register ~~first value has a greater number of bits than the first portion.~~

16. (cancelled)

17. (currently amended) The apparatus of claim ~~16~~ 15, wherein:

the control logic includes logic for first and second control flows;

the second control flow is to translate an initial graphics controller address and does not access the second table; and

the first control flow is to translate an initial bus controller address and access the second table.

18. (cancelled) .

19. (currently amended) A system, including:

a processor;

a memory;

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a graphics controller;
a bus controller;
an input-output controller coupled to the processor, memory, graphics controller
and bus controller, the input-output controller including :
a translation lookaside buffer coupled to an input register and an output
register;
control logic coupled to the translation lookaside buffer, the input register,
and the output register;
wherein the control logic is to compare a first portion of a first initial
address from the bus controller in the input register with entries in
the translation lookaside buffer; and if a first matching entry is
found, to combine a first value associated with the first matching
entry with a second portion of the first initial address to form a first
translated address having more bits than the first initial address and
hold the first translated address in the output register;
wherein the control logic is further to compare a first portion of a second
initial address from the graphics controller in the input register
with the entries in the translation lookaside buffer; and if a second
matching entry is found, to combine a second value associated
with the second matching entry with a second portion of the
second initial address to form a second translated address having
more bits than the second initial address and hold the second
translated address in the output register.

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20. (previously amended) The system of claim 19, wherein the control logic is further to:

access a table in memory if the first matching entry is not found;

find a third value in the table associated with the first portion of the first initial address;

combine the third value with the second portion of the first initial address to form a third translated address; and

hold the third translated address in the output register.

21. (previously amended) The system of claim 20, wherein:

the control logic includes logic for first and second control flows;

the second control flow is to translate an initial graphics controller address and does not access the table; and

the first control flow is to translate an initial bus controller address and access the table.

22-29. (cancelled)

30. (previously added) An apparatus comprising:

an address translator having a first interface to couple to a memory controller, a second interface to couple to a graphics controller, a third interface to couple to a bus controller, and a table of entries, each entry having a first portion and a second portion;